

Enhanced Test Condition

PSE Conformance Test Suite							802.3at Conformance Report								
May 8 2024 11:07 AM							version 5.3.14								
Port Count..... 5							Test Mode: 30 Watt PHYreport version 5.3.08								
Loop Count..... 1							Sifos Interop Index*: 100%								
PSE Tested: Unspecified Type-2 30W		Error Log: None													
Chassis ID: 192.168.221.105		PSA-3000 Ports								Low	P/F	High	P/F		
TestLoop: 1		1-1	1-1	1-1	1-1	1-1	UNITS	Min	Max	Average	Limit		Limit		
Test: det_v															
Open_Circuit_Det_Voc=		14.82	14.85	14.82	14.82	14.8	V	14.8	14.85	14.82	2.8	Pass	30	Pass	
Peak_Det_Vvalid=		6.25	6.25	6.25	6.25	6.25	V	6.25	6.25	6.3	3.8	Pass	10	Pass	
Min_Det_Vvalid=		4.18	4.18	4.18	4.18	4.18	V	4.18	4.18	4.2	2.8	Pass	9	Pass	
Det_Volt_Step_dVtest=		2.07	2.07	2.07	2.07	2.07	V	2.07	2.07	2.1	1	Pass	7.2	Pass	
Detection_Slew=		0	0	0	0	0	V/usec	0	0	0	0	Pass	0.1	Pass	
Good_Sig_Det_Pulse=		1	1	1	1	1	edges	1	1	1	1	Pass	9	Pass	
Backoff_Voltage=		0.8	0.8	0.8	0.8	0.8	V	0.8	0.8	0.8	0	Pass	2.8	Pass	
Non_802_Discr_?=		0	0	0	0	0	****	0	0	0	0	Pass	0	Pass	
Detect_Strategy=		0	0	0	0	0	****	0	0	0	0	Pass	2	Pass	
Test: det_i															
Init_Current_Isc=		0.16	0.16	0.16	0.16	0.16	mA	0.16	0.16	0.16	0	Pass	5	Pass	
Det_Current_Isc=		0.15	0.15	0.15	0.15	0.15	mA	0.15	0.15	0.15	0	Pass	5	Pass	

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Test: det_range													
Rgood_Max=	29	29	29	29	29	Kohm	29	29	29	26	Pass	32	Pass
Rgood_Min=	17	17	17	17	17	Kohm	17	17	17	16	Pass	19	Pass
Rmid_det=	29	29	29	29	29	Kohm	29	29	29	26	Pass	33	Pass
Cgood_Max=	0.1	0.1	0.1	0.1	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Rbad_Cbad_Stat=	0	0	0	0	0	****	0	0	0	0	Pass	0	Pass
4Pair_Pwr_?=	0	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Test: det_time													
Backoff_Time_Tdbo=	996	996	996	996	996	msec	996	996	996	-1	Pass	1500	Pass
Eff_Backoff_Tdbo_eff=	996	996	996	996	996	msec	996	996	996	-1	Pass	1500	Pass
Backoff_Type=	0	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Detection_Time_Tdet=	373	373	373	373	373	msec	373	373	373	5	Pass	500	Pass
Total_Det_Time=	377	377	377	377	377	msec	377	377	377	5	Pass	1000	Pass
Test: det_resource													
PSE_Detect_Source=	1	1	1	1	1	****	1	1	1	0	Pass	1	Pass
Output_Impedance_Zout=	450	450	450	450	450	Kohm	450	450	450	45	Pass	2000	Pass
Test: class_v													
Vclass_Max=	18.4	18.4	18.4	18.4	18.4	V	18.4	18.4	18.4	15.5	Pass	20.5	Pass
Vclass_Min=	18	17.5	18	18	18	V	17.5	18	17.9	15.5	Pass	20.5	Pass
Mark_Voltage_Vmark=	8.6	8.7	8.7	8.6	8.9	V	8.6	8.9	8.7	7	Pass	10	Pass
Mark_Voltage_Min=	8.6	8.6	8.6	8.6	8.6	V	8.6	8.6	8.6	7	Pass	10	Pass
Test: class_time													

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Class_0_Count=	1	1	1	1	1	****	1	1	1	1	Pass	2	Pass
Class_Time_Tpdc=	10.8	12.7	10.8	10.8	12.7	msec	10.8	12.7	11.6	6	Pass	75	Pass
Class_4_Count=	2	2	2	2	2	****	2	2	2	2	Pass	2	Pass
Event1_Tcle1=	11.7	11.7	11.7	11.7	13.6	msec	11.7	13.6	12.1	6	Pass	30	Pass
Event2_Tcle2=	11.7	11.7	9.7	9.7	11.7	msec	9.7	11.7	10.9	6	Pass	30	Pass
Mark_Tme1=	9.7	9.7	11.7	11.7	9.7	msec	9.7	11.7	10.5	6	Pass	12	Pass
Mark_Tme2=	253.1	253.1	255	255	253.1	msec	253.1	255	253.9	6	Pass	376	Pass
Mark_Tme1_LowI=	9.7	9.7	9.7	9.7	9.7	msec	9.7	9.7	9.7	6	Pass	12	Pass
Test: class_err													
Class_lim=	67	67	67	67	67	mA	67	67	67	51	Pass	100	Pass
Pwr_Cl_lim=	0	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Pwr_Cl_55=	0	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Mark_lim=	6	6	6	6	6	mA	6	6	6	5	Pass	100	Pass
Pwr_Cl_Uneven=	0	0	0	0	0	****	0	0	0	0	Pass	0	Pass
Treset=	213	213	213	213	213	msec	213	213	213	15	Pass	10000	Pass
Test: pwrup_time													
Power-On_Trise_c0=	144	147	147	144	147	usec	144	147	146	15	Pass	50000	Pass
Power-On_Tpon_c0=	271.5	271.5	271.5	269.5	271.5	msec	269.5	271.5	271.1	0	Pass	400	Pass
Power-On_Trise_c4=	161	164	164	165	165	usec	161	165	164	15	Pass	50000	Pass
Power-On_Tpon_c4=	293	293	293	293	289.1	msec	289.1	293	292.2	0	Pass	400	Pass
Test: pwrup_inrush													
Init_Iinrush=	424	423.88	423.38	423.5	423.5	mA	423.38	424	423.7	400	Pass	450	Pass

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Max_Iinrush_c0=	418.75	419	419	418.88	418.88	mA	418.75	419	418.9	400	Pass	450	Pass
Max_Iinrush_c4=	418.75	418.88	418.88	419.25	418.75	mA	418.75	419.25	418.9	400	Pass	450	Pass
Min_Iinrush=	409.5	409.5	409.63	409.63	408.75	mA	408.75	409.63	409.4	400	Pass	450	Pass
Tinrush=	60	60	60	60	60	msec	60	60	60	50	Pass	75	Pass
Inrush_45m=	53.8	53.8	53.8	53.8	53.8	V	53.8	53.8	53.8	50	Pass	57	Pass
Inrush_Voltage=	30.5	30.5	30.5	30.5	30.5	V	30.5	30.5	30.5	30	Pass	57	Pass
Inrush_Strategy_c0=	0	0	0	0	0	****	0	0	0	0	Pass	1	Pass
Inrush_Strategy_c4=	0	0	0	0	0	****	0	0	0	0	Pass	1	Pass
Test: pwr on_v													
Vport_min=	53.3	53.3	53.3	53.3	53.3	V	53.3	53.3	53.3	50	Pass	57	Pass
Vport_max=	54.2	54.2	54.2	54.2	54.2	V	54.2	54.2	54.2	50	Pass	57	Pass
Vport_ripple=	417	416	416	417	416	mVpp	416	417	416.4	0	Pass	500	Pass
Vport_noise=	37	36	38	38	37	mVpp	36	38	37.2	0	Pass	200	Pass
Vtrans_min=	52.2	52.2	52.2	52.2	52.2	V	52.2	52.2	52.2	50	Pass	57	Pass
Vtrans_max=	54.3	54.4	54.3	54.3	54.3	V	54.3	54.4	54.3	50	Pass	57	Pass
Test: pwr on_pwr cap													
Pcon_c0=	18.5	18.5	18.5	18.5	18.5	W	18.5	18.5	18.5	14.2	Pass	22.7	Pass
Icon_%_c0=	134	134	134	134	134	%	134	134	134	100	Pass	9999	Pass
Pcon_c1=	5.7	4.6	5.7	5.7	5.7	W	4.6	5.7	5.5	3.9	Pass	22.7	Pass
Icon_%_c1=	147	116.7	147	147	147	%	116.7	147	140.9	100	Pass	9999	Pass
Pcon_c2=	8.2	8.2	8.2	8.2	8.2	W	8.2	8.2	8.2	6.8	Pass	22.7	Pass
Icon_%_c2=	122.2	122.2	122.2	122.2	122.2	%	122.2	122.2	122.2	100	Pass	9999	Pass

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Pcon_c3=	18.5	18.5	18.5	18.5	18.5	W	18.5	18.5	18.5	14.2	Pass	22.7	Pass
Icon_%_c3=	134	134	134	134	134	%	134	134	134	100	Pass	9999	Pass
Pcon_c4=	34	34	34	34	34	W	34	34	34	28.7	Pass	38.9	Pass
Icon_%_c4=	116.2	116.2	116.2	116.2	116.2	%	116.2	116.2	116.2	100	Pass	9999	Pass
Type-2_Enable=	1	1	1	1	1	****	1	1	1	1	Pass	1	Pass
Test: pwrn_maxi													
Ilim_Peak_1=	479	478	477.5	475.8	477.5	mA	475.8	479	477.6	0	Pass	1750	Pass
Ilim_Min_1=	403.4	403.6	403.5	403.6	403.6	mA	403.4	403.6	403.5	400	Pass	1750	Pass
Tlim_1=	62.1	61.7	62.1	61.7	61.3	msec	61.3	62.1	61.8	10	Pass	9999	Pass
Vlim_1=	53.4	53.4	53.4	53.4	53.4	V	53.4	53.4	53.4	50	Pass	57	Pass
Ilim_Max_1=	482.8	480.3	481.8	481	480.3	mA	480.3	482.8	481.2	400	Pass	1750	Pass
Ktran_lo_1=	106.5	106.6	106.8	107	106.7	%	106.5	107	106.7	92.4	Pass	115	Pass
Ilim_Peak_2=	844.5	842.8	843.3	841.8	840.8	mA	840.8	844.5	842.6	0	Pass	1750	Pass
Ilim_Min_2=	687	686.9	686.9	687	687	mA	686.9	687	687	683	Pass	1750	Pass
Tlim_2=	36.3	61.3	62.1	61.7	61.3	msec	36.3	62.1	56.5	10	Pass	75	Pass
Vlim_2=	52.9	52.9	52.9	52.9	52.9	V	52.9	52.9	52.9	50	Pass	57	Pass
Ilim_Max_2=	827.5	826.8	828	825.8	826.5	mA	825.8	828	826.9	683	Pass	1750	Pass
Ktran_lo_2=	105.5	105.3	106	106	105.9	%	105.3	106	105.7	92.4	Pass	115	Pass
Test: pwrn_overld													
%Ipeak_1=	125	125	125	125	125	%	125	125	125	100	Pass	125	Pass
Vport_Ipeak_1=	53.4	53.4	53.4	53.4	53.4	V	53.4	53.4	53.4	50	Pass	57	Pass
Vport_5%DC_1=	53.4	53.5	53.4	53.4	53.5	V	53.4	53.5	53.4	50	Pass	57	Pass

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%Ipeak_2=	106.4	106.4	125	125	103.2	%	103.2	125	113.2	100	Pass	125	Pass
Vport_Ipeak_2=	52.9	52.9	52.9	53	53	V	52.9	53	52.9	50	Pass	57	Pass
Vport_5%DC_2=	53	53	53	53	53	V	53	53	53	50	Pass	57	Pass
Test: mps_dc_valid													
Min_Valid_Time_Tmps=	10	10	10	10	10	msec	10	10	10	1	Pass	60	Pass
Duty_Cycle_tol=	1	1	1	1	1	****	1	1	1	1	Pass	1	Pass
Test: mps_dc_pwrdsn													
Min_Valid_I_hold=	6	6	6	6	6	mA	6	6	6	5	Pass	10	Pass
Time-to-Shutdown_Tmpdo=	361	361	361	361	361	msec	361	361	361	300	Pass	400	Pass
Test: pwrdsn_overld													
Icut_1=	382	382	382	382	382	mA	382	382	382	-1	Pass	1750	Pass
Tcut_1=	61.2	61.6	62.1	61.1	61.6	msec	61.1	62.1	61.5	50	Pass	9999	Pass
Isoft_1=	-1	-1	-1	-1	-1	mA	-1	-1	-1	-1	Pass	683	Pass
Tsoft_1=	-1	-1	-1	-1	-1	msec	-1	-1	-1	-1	Pass	2000	Pass
Icut_2=	644.3	644.3	644.3	644.3	644.3	mA	644.3	644.3	644.3	-1	Pass	1750	Pass
Tcut_2=	62	61.3	62	62	61.7	msec	61.3	62	61.8	10	Pass	9999	Pass
Isoft_2=	-1	-1	-1	-1	-1	mA	-1	-1	-1	-1	Pass	683	Pass
Tsoft_2=	-1	-1	-1	-1	-1	msec	-1	-1	-1	-1	Pass	2000	Pass
Test: pwrdsn_time													
Turn-Off_Time_Toff=	52.2	52.3	52.5	52.6	52.6	msec	52.2	52.6	52.4	0	Pass	500	Pass
Output_Cap_Cout=	0.0589	0.059	0.0592	0.0593	0.0594	uF	0.0589	0.0594	0.06	-1	Pass	0.52	Pass
Output_Load_Rp=	9999	9999	9999	9999	9999	Kohm	9999	9999	9999	45	Pass	50000	Pass

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Test: pwrdn_v													
Avg_Idle_Voff=	0.7	0.7	0.7	0.8	0.7	V	0.7	0.8	0.7	0	Pass	2.8	Pass
Error_Delay_Ted=	1835.9	3687.5	3484.4	1648.4	1648.4	msec	1648.4	3687.5	2461	750	Pass	10000	Pass
Peak_Error_Delay_Ved=	0.9	18.1	18.1	0.9	0.9	V	0.9	18.1	7.8	0	Pass	20.5	Pass
Test Port Model Number:	3202	3202	3202	3202	3202								
Test Port Hardware Version:	11	11	11	11	11								
Test Port Firmware Version:	4.19 lc19	4.19 lc19	4.19 lc19	4.19 lc19	4.19 lc19								